



EW CFC #10 ECU

TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application Number	09/998,420 (U.S. Patent No. 6,552,394 B2)
	Filing Date	November 29, 2001 (issued April 22, 2003)
	First Named Inventor	Aftab Ahmad et al.
	Art Unit	2811
	Examiner Name	On Nadav
Total Number of Pages in This Submission	Attorney Docket Number	MI22-1885

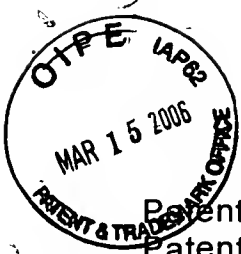
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Firm Name	Wells St. John P.S.	MAR 20 2006
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Printed name	James E. Lake	
Date	13 Mar 2006	Reg. No. 44,854

CERTIFICATE OF TRANSMISSION/MAILING		
I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:		
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MAR 27 2006



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent No. 6,552,394 B2
Patent Issue Date April 22, 2003
Application Serial No. 09/998,420
Filing Date November 29, 2001
Assignee Micron Technology, Inc.
Inventorship Aftab Ahmad et al.
Attorney's Docket No. MI22-1885
Title: Semiconductor Transistor Devices and Structures with Halo Regions

REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT
FOR PTO MISTAKE (37 C.F.R. 1.322(a))

To: Commissioner for Patents
P.O. Box 1450
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ATTN: Decision and Certificate of Correction
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From: James E. Lake (Tel. 509-624-4276; Fax 509-838-3424)
Wells St. John P.S.
601 W. First Avenue, Suite 1300
Spokane, WA 99201-3828

Sir:

It is hereby requested that a Certificate of Correction be issued with respect to Patent No. 6,552,394 B2, granted April 22, 2003, in accordance with the Certificate of Correction form attached hereto in duplicate.

The errors listed on the Certificate of Correction form were apparently incurred through the fault of the PTO as will be disclosed by the records of files in the Office.

Since this Certificate of Correction is being requested due to PTO errors, it is believed that no fee is due. However, in the event that a fee is required for issuance of this Certificate of Correction, please charge the fee specified under

MAR 27 2006

37 C.F.R. § 1.20(a) to Deposit Account No. 23-0925. Please credit Deposit Account No. 23-0925 with any overpayment of the above fee.

Corrections to the drawings were requested in the Letter Submitting Formal Drawings, filed November 28, 2001, and the annotated drawings that accompanied it. Fig. 29 has not been corrected pursuant to the letter and drawings submitted on November 28, 2001.

Attached hereto, in duplicate is Form PTO-1050, with at least one copy being suitable for printing.

Respectfully submitted,

Dated: 13 Mar 2006

By:

James E. Lake
James E. Lake
Reg. No. 44,854

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,552,394 B2
DATED : April 22, 2003
INVENTOR(S) : Aftab Ahmad et al.

Page 1 of 2

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Drawings.

Fig. 18, replace "56" with -- 54 --.

Fig. 21, replace "56" with -- 54 --.

Column 1.

Lines 6-10, delete in their entirety.

Column 10.

Line 53, replace "transistor By device **105** and an array of NMOS memory" with
-- transistor device **105** and an array of NMOS memory --.

Column 13.

Line 39, replace "and is implanted under the either the conditions described" with
-- and is implanted under either of the conditions described --.

Column 15.

Line 34, replace "form of an array of NMOS memory transistors **303** with" with
-- form an array of NMOS memory transistors **303** with --.

Column 16.

Line 18, replace "about 1×10^{12} atoms/cm² to about 1×10^{12} atoms/cm² and at" with
-- about 1×10^{12} atoms/cm² to about 1×10^{13} atoms/cm² and at --.

Column 17.

Line 18, replace "an insulating layer complicates later processes forming" with
-- an insulating layer complicates later processing of forming --.

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,552,394 B2
DATED : April 22, 2003
INVENTOR(S) : Aftab Ahmad et al.

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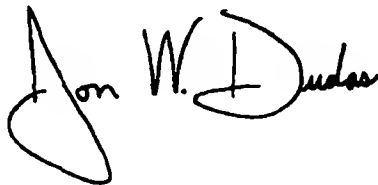
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 17 (cont'd).

Line 42, replace "Referring to FIG. 34, a dopant 358 is implanted an angle" with
-- Referring to FIG. 34, a dopant 358 is implanted at an angle --.

Signed and Sealed this

Twenty-first Day of February, 2006

A handwritten signature in black ink, appearing to read "Jon W. Dudas". The signature is stylized with a large, looped initial "J" and a distinct "D" at the end.

JON W. DUDAS
Director of the United States Patent and Trademark Office

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

Page 1 of 1

PATENT NO. : US 6,552,394 B2

APPLICATION NO.: 09/998,420

DATED : April 22, 2003

INVENTOR(S) : Aftab Ahmad et al.

It is certified that an error or errors appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Sheet 15 of 20, Fig. 29

Replace the number "307" under number 274

With the number --311-- under number 274

Mailing Address of Sender:

James E. Lake
Wells St. John P.S.
601 West First Avenue, Suite 1300
Spokane, WA 99201-3828

Patent No. US 6,552,394 B2



11/29/2001

MT22-1485

Micron Technology, Inc.

The stamp of the U.S. Patent and Trademark Office acknowledges receipt of the application for letters patent of the following

Applicant: Aftab Ahmad, et al

Titled: "Semiconductor Transistor Devices and Methods for Forming Semiconductor Transistor Devices"

1. Return Postcard Receipt;
2. A \$740.00 check;
3. PTO Utility Application Transmittal Form (PTO/SF/05);
4. Fee Transmittal Form (PTO/SF/17);
5. Ninety-three (93) pages of Specification, Claims and Abstract plus title page; **20 pgs of as filed drawings Figs. 1-38**
6. Inventors Declaration (copy from parent case);
7. Letter submitting formal drawings;
8. Twenty (20) sheets of formal drawings (Figs. 1-38);
9. Preliminary Amendment
10. Information Disclosure Statement including PTO-1449.
11. 12 sheets of redline drawings
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